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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,778	03/31/2004	Kiyoshi Mita	14225-048001 / F1040146US	5229

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EXAMINER	
VAN, LUAN V	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,778	MITA, KIYOSHI	
	Examiner	Art Unit	
	Luan V. Van	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment of March 30, 2006 does not render the application allowable.

Status of Objections and Rejections

All rejections from the previous office action are maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tashiro.

Tashiro teaches a method for manufacturing a mounting substrate or circuit device 5 (figures 1-2), comprising: providing electrodes (i.e. , die pad 1 and bonding pads 2, figure 1) which are arranged in plurality of rows (two vertical rows and two horizontal rows of bond pads, figure 1) to surround a circuit element disposed in the vicinity of a center part (die pad 1 and bonding pads 2, figure 1, are in the vicinity of a center) of a mounting substrate and directly electrically interconnecting the adjacent electrodes to each other by use of plating wires 3 (figure 1); energizing the electrodes

via the plating wires to coat the electrodes with plated films by electroplating (column 3 lines 37-51); electrically separating the individual electrodes from each other by cutting off the plating wires (column 3 lines 45-51); fixing a circuit element on the mounting substrate (column 3 line 65 -- column 4 line 4) and electrically connecting the electrodes to the circuit element (column 3 line 65 -- column 4 line 4); and forming a sealing resin to cover the circuit element (column 4 lines 5-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro in view of Kado et al.

Tashiro teaches the method as described above. Additionally, Tashiro teaches that the wiring board is a double-face mounted multilayer wiring board (column 4 lines

20-25). Each side of the wiring board contains bonding pads and die pads as shown in figures 1 and 2. The reference to Tashiro differs from the instant claims in that the reference does not explicitly teach electrically connecting the front face electrodes to the back face electrodes (claims 3 and 8); placing the electrodes in a matrix form (claims 4 and 9); nor dicing as the means for cutting the wires (claims 5 and 10).

Kado et al. teach a mounting substrate where the lower surface (or back face) has a plurality of electrode pads arranged in an array form, wherein the electrode pads are electrically connected to the wiring lines (paragraph 77), which are electrically connected to the front face electrodes (paragraph 75). Solder bumps are applied to the electrode pads which constitute external connection terminals of the multi-chip module (paragraph 77). Kado et al. also teach that the electrodes are arranged in a matrix form as shown in figure 3, and that the multi-wiring substrate is cut by dicing to form individual pieces that are electrically isolated from each other (paragraph 81).

Addressing claims 3 and 8, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Tashiro by electrically connecting the front face electrodes and the back face electrodes as taught by Kado et al., because connecting the front face electrodes to the back face electrodes allows the mounted chip to be electrically connected to an external wiring substrate of an electronic device.

Addressing claims 4 and 9, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Tashiro by arranging the electrodes in a matrix form as taught by Kado et al., because

such arrangement would provide a larger area for mounting electronic components and contribute to the improvement of the mounting density of the board.

Addressing claims 5 and 10, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Tashiro by dicing as a means for cutting as taught by Kado et al., because dicing is a suitable process for cutting a wiring substrate.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive.

In the arguments presented on page 5 of the amendment, the applicant argues that Tashiro does not disclose the electrodes being directly interconnected. The examiner respectfully disagrees. The bonding pads 2 of Tashiro are directly interconnected by the fine line pattern 3. However, even in the absence of fine line pattern 3, the bonding pads 2 of Tashiro are directly electrically interconnected through die pad 1. Furthermore, the applicant appears to be arguing a different interpretation of the claims. The claims recite that the electrodes are "directly electrically interconnected", which has a different meaning from "directly interconnected". The claims are broadly interpreted to reflect the recited limitations in the instant claims.

In the arguments presented on page 6 of the amendment, the applicant argues that it would not be possible to provide electrical connection externally to the electrode of the wiring board of Tashiro due to the covering resin. The examiner respectfully disagrees. Tashiro discloses that the electronic components, i.e. IC chip, are mounted

on the wiring board which is subjected to a wire bonding process prior to applying the resin coating (column 4 lines 1-12). However, even assuming this is not the case, it would have been obvious to one having ordinary skill in the art to form the external electrical connections to the electrode prior to applying the resin coating, because the resin coating is electrically insulating.

The applicant further argues that it would not have been obvious to have modified the method of Tashiro by using the dicing means for cutting as taught by Kado et al., because Kado et al. teach dicing to form entirely separate package substrates. The examiner respectfully disagrees. First, Tashiro already teaches cutting the fine line pattern without cutting through the substrate. Second, Kado et al. teach cutting the wiring lines without cutting off the substrate completely (paragraph 84).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan V. Van whose telephone number is 571-272-8521. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LVV
April 24, 2006

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700